ABSTRACT OF THE DISCLOSURE

A SRAM device is provided having a plurality of memory cells. Each memory cell may include a plurality of transistors coupled in a cross-coupled inverter configuration. An NMOS transistor may be coupled to a body of the two PMOS transistors in the cross-coupled inverter configuration so as to apply a forward body bias to the PMOS transistors of the cross-coupled inverter configuration. A power control unit may control a supply voltage to each of the PMOS transistors as well as apply the switching signal to the NMOS transistor based on a STANDBY mode of the memory cell.